

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A method in a data processing system for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the method comprising:
responsive to loading an instruction in the code into a cache, determining, by a processor unit, whether a prefetch indicator is associated with the instruction; and
responsive to the prefetch indicator being associated with the instruction, selectively prefetching a pointer to a data structure identified by the prefetch indicator into the cache in the processor.
2. (Original) The method of claim 1, wherein the prefetch indicator contains the pointer to the data structure.
3. (Original) The method of claim 1, wherein the selectively prefetching step includes: determining whether outstanding cache misses are present; and
prefetching the data if a number of outstanding cache misses are less than a threshold.
4. (Original) The method of claim 1, wherein the selectively prefetching step includes:
determining whether to replace cache lines; and
prefetching the data if a number of cache lines chosen to be replaced are greater than a threshold.
5. (Original) The method of claim 1, wherein the processor unit is selected from one of an instruction cache, data cache, or a load/store unit.
6. (Original) The method of claim 1, wherein the cache is an instruction cache.
7. (Original) The method of claim 1, wherein the cache is a data cache.

8. (Original) A data processing system comprising:
a cache in a processor in the data processing system; and
a load/store unit in the processor, wherein the load/store unit determines whether a prefetch indicator is associated with an instruction in response to loading the instruction for execution into the cache, the load/store unit selectively prefetches a pointer to a data structure identified by the prefetch indicator into the cache using metadata associated with the instruction.
9. (Original) The data processing system of claim 8, wherein the cache is at least one of an instruction cache and a data cache.
10. (Original) The data processing system of claim 8, wherein the load/store unit selectively prefetches the pointer to the data structure based on a determination by the cache as to whether the prefetch is to occur.
11. (Original) A data processing system for providing hardware assistance to prefetch data during execution of code by a process or in the data processing system, the data processing system comprising:
determining means, responsive to loading an instruction in the code into a cache, for determining, by the a processor unit, whether a prefetch indicator is associated with the instruction; and
selectively prefetching means, responsive to the prefetch indicator being associated with the instruction, for selectively prefetching a pointer to a data structure identified by the prefetch indicator into the cache in the processor.
12. (Original) The data processing system of claim 11, wherein the prefetch indicator contains the pointer to the data structure.
13. (Original) The data processing system of claim 11, wherein the selectively prefetching means includes:
means for determining whether outstanding cache misses are present; and
means for prefetching the data if a number of outstanding cache misses are less than a threshold.

14. (Original) The data processing system of claim 11, wherein the selectively prefetching means includes:
- means for determining whether to replace cache lines; and
 - means for prefetching the data if a number of cache lines chosen to be replaced are greater than a threshold.
15. (Original) The data processing system of claim 11, wherein the processor unit is selected from one of an instruction cache, a data cache, or a load/store unit.
16. (Original) The data processing system of claim 11, wherein the cache is an instruction cache.
17. (Original) The data processing system of claim 11, wherein the cache is a data cache.
18. (Currently amended) A computer program product in a recordable-type computer readable medium for providing hardware assistance to prefetch data during execution of code by a process or in the data processing system, the computer program product comprising:
- first instructions, responsive to loading an instruction in the code into a cache, for determining, by the a processor unit, whether a prefetch indicator is associated with the instruction; and
 - second instructions, responsive to the prefetch indicator being associated with the instruction, for selectively prefetching a pointer to a data structure identified by the prefetch indicator into the cache in the processor.
19. (Original) The computer program product of claim 18, wherein the prefetch indicator contains the pointer to the data structure.
20. (Original) The computer program product of claim 18, wherein the second instructions includes:
- first sub-instructions for determining whether outstanding cache misses are present; and
 - second sub-instructions for prefetching the data if a number of outstanding cache misses are less than a threshold.
21. (Original) The computer program product of claim 18, wherein the second instructions includes:
- first sub-instructions for determining whether to replace cache lines; and
 - second sub-instructions for prefetching the data if a number of cache lines chosen to be replaced are greater than a threshold.

22. (Original) The computer program product of claim 18, wherein the processor unit is selected from one of an instruction cache, a data cache, or a load/store unit.
23. (Original) The computer program product of claim 18, wherein the cache is an instruction cache.
24. (Original) The computer program product of claim 18, wherein the cache is a data cache.